Doc code :IDS
Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (09-08)
Approved for use through 10/31/2008. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	10544894
Filing Date	2006-07-19
First Named Inventor	Dasu, Aravind R.
Art Unit	2193
Examiner Name	Bullock,Jr., Lewis Alexander
Attorney Docket Number	117316-155055

U.S.PATENTS Remove

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1					

If you wish to add additional U.S. Patent citation information please click the Add button. Add

U.S.PATENT APPLICATION PUBLICATIONS Remove

Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1					

If you wish to add additional U.S. Published Application citation information please click the Add button. Add

FOREIGN PATENT DOCUMENTS Remove

Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] ¡	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1							☐

If you wish to add additional Foreign Patent Document citation information please click the Add button Add

NON-PATENT LITERATURE DOCUMENTS Remove

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	10544894
	Filing Date	2006-07-19
	First Named Inventor	Dasu, Aravind R.
	Art Unit	2193
	Examiner Name	Bullock,Jr., Lewis Alexander
	Attorney Docket Number	117316-155055

	1	Fredriksson, Kimmo " Faster String Matching with Super-Alphabets" Proc of SPIRE' 2002, Lecture Notes in Computer Science 2476, pages 44-57, Springer Verlag, Berlin 2002	☐
	2	George, V.,et al. " The Design of a Low Energy FPGA", International Symposium on Low Power Electronics and Design, 1999	☐
	3	Gold, S., et al. " A Graduated Assignment Algorithm for Graph Matching" IEEE Trans. On Pattern Analysis and Machine Intelligence, Vol. 18, NO. 4, April 1996	☐
	4	Goldstein, S., et al. " PipeRench: A Coprocessor for Streaming Multimedia Acceleration" Carnegie Mellon University	☐
	5	Gupta, R., et al. " A Co-Synthesis Approach to Embedded System Design Automation" Design Automation for Embedded Systems, V1 N1/2, 1996, 69-120	☐
	6	Hadlock, F. "Finding A Maximum Cut of A Planar Graph In Polynomial Time" SIAM Journal of Computing, 4, no. 3:331-225, Sept. 1975	☐
	7	Hartenstein, R., et al. " KressArray Xplorer: A New CAD Environment to Optimize Reconfigurable Datapath Array Architectures" Proc of the ASP-DAC Asia and South Pacific Design Automation Conference, 2000	☐
	8	Hopcroft, J.E., et al. " Linear Time Algorithm for Isomorphism of Planar Graphs" Sixth ACM Symposium on Theory of Computing, 1974	☐
	9	Huang, L., et al. "An Approach to Distribution of Parallel Programs With Conditional Task Attributes" Technical Report TR97-06, Department of Computer Science, The University of Adelaide, August, 1997	☐
	10	Huang, L., et al. "Design an Implementation of an Adaptive Task Mapping Environment for Parallel Programming" Australian Computer Science Communications, 19 (1) 326-335, February, 1997	☐
	11	Hwu, W., et al. " The Superblock: An Effective Technique for VLIW and Superscalar Compilation" Journal of Supercomputing, 7: 229-248 (1993)	☐

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	10544894
	Filing Date	2006-07-19
	First Named Inventor	Dasu, Aravind R.
	Art Unit	2193
	Examiner Name	Bullock,Jr., Lewis Alexander
	Attorney Docket Number	117316-155055

	12	Iseli, C. et al. " A C ++ Compiler for FPGA Custom Execution Units Synthesis" IEEE Symposium on FPGAs for Custom Computing Machines, 1995	☐
	13	ISO/IEC JTC1/SC29/WG11 N3908 "MPEG-4 Video Verification Model version 18.0" January 2001	☐
	14	Jain, S., et al. "Speeding Up Program Execution Using Reconfigurable Hardware and a Hardware Function Library" VLSI Design, 1998 Proceedings, 1998 Eleventh International Conference, IEEE 1997/1998, pp. 400-405	☐
	15	Janssen, M., et al. " A Specification Invariant Technique for Regularity Improvement between Flow-Graph Clusters" IEEE Proceedings of the 1996 European Design and Test Conference (ED&TC), pages 138-143 (1996)	☐
	16	Jiajun, Y., et al. " A Fuzzy Expert System Architecture Implementing Onboard Planning and Scheduling for Autonomous Small Satellite" 12th Annual AIAA/Utah State University Conference on Small Satellites, Logan, Utah, August 1998	☐
	17	Jung, Sung-Hwan " Content-based Image Retrieval Using Fuzzy Multiple Attribute Relational Graph" IEEE International Symposium on Industrial Electronics Proceedings (ISIE 2001), 3: 1508-1513, 2001	☐
	18	Kasahara, H., et al. " Practical Multiprocessor Scheduling Algorithms for Efficient Parallel Processing" IEEE Trans. On Comp., V33, Nul 1, 1984, 1023-1029	☐
	19	Kastner, R. et al."Instruction Generation for Hybrid Reconfigurable Systems" International Conference on Computer-Aided Design (ICCAD), November, 2001	☐
	20	Kastrup, B. et al. "ConCISe: A Compiler-Driven CPLD-Based Instruction Set Accelerator" IEEE Symposium on Field Programmable Custom Computing Machines, 1999	☐
	21	Keutzer, Kurt "DAGON: Technology Binding and Local Optimization by DAG Matching" Proc. Of Design Automation Conference, 1987	☐
	22	Ku, D., et al. " Relative Scheduling under Timing Constraints" IEEE Trans. Computer-Aided Design, Vol. 11, pp. 696-718, June, 1992	☐

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	10544894
	Filing Date	2006-07-19
	First Named Inventor	Dasu, Aravind R.
	Art Unit	2193
	Examiner Name	Bullock,Jr., Lewis Alexander
	Attorney Docket Number	117316-155055

	23	Kuramochi, M., et al. " An Efficient Algorithm for Discovering Frequent Subgraphs" Technical Report 02-026, University of Minnesota, 2002	☐
	24	Kwok, Y.K., et al. " Dynamic Critical-Path Scheduling: An Effective Technique for Allocating Task Graphs to Multiprocessors" IEEE Transactions on Parallel and Distributed Systems, Vol. 7, NO 5, May 1996 pp. 506-521	☐
	25	Lai, Y.T., et al. "Hierarchical Interconnection Structures for Field Programmable Gate Arrays" IEEE Transactions on Very Large Scale Integration (VSLI) Systems, Vol. 5. No 2, pp. 186-196, June 1997	☐
	26	Lakshminarayana, G., et al. " Wavesched: A Novel Scheduling Technique for Control-Flow Intensive Designs" IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Vol. 18, No. 5, May, 1999	☐
	27	Lee, W. et al. "Space-Time Scheduling of Instruction-Level Parallelism on a Raw Machine", Proc of the Eighth International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS), San Jose, CA, October 1998	☐
	28	Li, S., et al. " Configuration Code Generation and Optimizations for Heterogeneous Reconfigurable DSPS" Proceedings of SIPS99	☐
	29	Li, W., et al. "Routability Prediction for Hierarchical FPGAs" Ninth Great Lakes Symposium on VLSI, pp. 256-259, 4-6 March 1999	☐
	30	Liu, J. et al. " Variable Instruction Set Architecture and Its Compiler Support" IEEE Transactions on Computers, 2003	☐
	31	Marquardt, A, et al. "Using Cluster-Based Logic Blocks and Timing-Driven Packing to Improve FPGA Speed and Density" Proceeding of the 1999 ACM/SIGDA Seventh International Symposium on Field Programmable Gate Arrays, p. 37-46, February 21-23, 1999, Monterey	☐
	32	Marshall, T. et al. " A Reconfigurable Arithmetic Array for Multimedia Applications" Proc of the ACM/SIGDA Seventh International Symposium on Field Programmable Gate Arrays, 1999	☐
	33	Messmer, B.T., et al. " A decision tree approach to graph and subgraph isomorphism detection" Pattern Recognition, 32: 1979-1998, 1999	☐

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	10544894
	Filing Date	2006-07-19
	First Named Inventor	Dasu, Aravind R.
	Art Unit	2193
	Examiner Name	Bullock,Jr., Lewis Alexander
	Attorney Docket Number	117316-155055

	34	Mirsky, E. et al. " MATRIX: A Reconfigurable Computing Architecture with Configurable Instruction Distribution and Deployable Resources" IEEE Symposium on FPGAs for Custom Computing Machines, April 17-19, 1996, Napa, CA	☐
	35	Miyamori, T., et al. " A Quantitative Analysis of Reconfigurable Coprocessors for Multimedia Applications" IEEE Symposium on FPGAs for Custom Computing Machines, 1998	☐
	36	Mohamed, A., et al. "Hardware Implementation of Phong Shading using Spherical Interpolation" Periodica Polytechnica, Vol. 44, Nos 3-4, 2000	☐
	37	Mooney, Vincent J. III " Path-Based Edge Activation for Dynamic Run-Time Scheduling" International Symposium on System Synthesis (ISSSS'99), pp. 30-36, November, 1999	☐
	38	Moreano, J., et al. " Datapath Merging and Interconnection Sharing for Reconfigurable Architectures" ACM ISSS'02, pages 38-43 (2002)	☐
	39	Moreno, J.M. et al. "Approaching Evolvable Hardware to Reality: The Role of Dynamic Reconfiguration and Virtual Meso-structures" Microelectronics for Neural, Fuzzy and Bio-Inspired Systems, 1999	☐
	40	Nagaraj, Raghavendra C. " Complexity Analysis of MPEG- 4 Video Object Profiles" A Masters Thesis, Arizona State University, 2000	☐
	41	Perchant, A., et al. " A New Definition for Fuzzy Attributed Graph Homomorphism with Application to Structural Shape Recognition in Brain Imaging" hi IMTC'99, 16th IEEE Instrumentation and Measurement Technology Conference, pages 1801-1806 Venice, Italy, May, 1999	☐
	42	Rabaey, Jan M. "Reconfigurable Processing: The Solution to Low-Power Programmable DSP" Proceedings 1997 ICASSP Conference Munich April 1997	☐
	43	Rangarajan, A., et al. " A Lagrangian Relaxation Network for Graph Matching" IEEE Transactions on Neural Networks, 7 (6): 1365-1381, 1996	☐
	44	Rao, D., et al. "On Clustering for Maximal Regularity Extraction" IEEE Transactions on Computer-Aided Design, Vol. 12, No. 8, August, 1993	☐

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	10544894
	Filing Date	2006-07-19
	First Named Inventor	Dasu, Aravind R.
	Art Unit	2193
	Examiner Name	Bullock,Jr., Lewis Alexander
	Attorney Docket Number	117316-155055

	45	Rewini, H., et al. "Static Scheduling of Conditional Branches in Parallel Programs" Journal of Parallel and Distributed Computing, 24, 4154 (1995)	☐
	46	Reyner, Steven W. " An Analysis of a Good Algorithm for the Subtree Problem" SIAM Journal of Computing, 6 (4): 730-732, 1997	☐
	47	Sarrigeorgidis, K., et al. "Massively Parallel Wireless Reconfigurable Processor Architecture and Programming" IOtlz Reconfigurable Architectures Workshop, Nice, France, April 22, 2003	☐
	48	Sawitzki, S. et al. "CoMPARE: A Simple Reconfigurable Processor Architecture Exploiting Instruction Level Parallelism" Proc. Of PART, pp.213-224, Springer-Verlag, 1998	☐
	49	Schoner, B., et al. " Issues in Wireless Video Coding using Run-Time-reconfigurable FPGAs" Proc of the IEEE Symposium on FPGAs for Custom Computing Machines, Napa CA, April 19-21, 1995	☐
	50	Singh, A., et al. " Efficient circuit Clustering for Area and Power Reduction in FPGAs" ACM Transactions on Design Automation of Electronic Systems, Volume 7, Issue 4, October 2002, pp. 643-663	☐

If you wish to add additional non-patent literature document citation information please click the Add button Add

EXAMINER SIGNATURE

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.